TAMILNADU STATE COUNCIL FOR SCIENCE AND TECHNOLOGY

DOTE Campus, Chennai-600025

STUDENT PROJECTS SCHEME

Proposals invited for 2019-2020

Tamilnadu State Council for Science and Technology has been implementing Student Projects Scheme in order to harness the talent and potential available with students for the benefit of our State. Under this scheme final year UG students (Engineering) / PG Science Students / PG professional Students who have dissertation work in their curriculum may apply. Financial support up to a maximum of Rs.10, 000/- will be provided to each project. Those who want to apply under this scheme are requested to read the instructions carefully and apply only in the prescribed format. The format and instructions in which the proposals are to be submitted is available in the Council's website. **(www.tanscst.nic.in).**

Two copies of proposals complete in all aspects are to be submitted through proper channel to **The Member Secretary, Tamilnadu State Council for Science and Technology, DOTE Campus, Chennai - 600 025** on or before **24 SEPTEMBER 2019, 5 pm.**

Instructions

1. The scheme is instituted for the purpose of providing assistance in the form of grant to **final year** students of **UG/PG (Engineering-Civil: Mechanical: :EEE/ECE/EIE/ICE:CSE/IT/Computer Application / Software : Chemical), PG (Professional Courses) and PG (all Sciences)** for scientific research work, with particular relevance to the State of Tamilnadu, for economic and industrial development.
2. Student projects will be eligible for a **maximum grant of Rs.10, 000/-.**
3. **Any One** sector in format (at Sl.NO.4) must be chosen and filled carefully. Incorrect filling or filling more than one sector will lead to rejection of your application.
4. The project team (batch) can have up to a maximum of four students. The project team should send only one proposal.
5. It may be noted that the project proposal should be of original, innovative and novel. They should have utility and applicability for implementation. Kindly note that the evaluation of the project is also based on these factors.
6. The Project Guides / HODs needs to evaluate the project proposals and scrutiny them before sending the project proposals to TNSCST.

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7. The project team **should not** change the topic and should not deviate from the objectives of the sanctioned project proposal. In the event of any such changes, grant will be treated as cancelled and the institution should return the sanctioned amount to TNSCST.

8. Project proposals received will be reviewed and evaluated by a team of experts and those selected will be announced in TNSCST website www.tanscst.nic.in. The project sanction letter and the money will be sent to the Principal/Registrar of the institution with a copy to the Project guide.

9. The sanctioned projects should be completed and the report should be submitted before end of **April 2020**.

10. The Utilization Certificate (UC) and Statement of Expenditure (SE) should be signed by the guide, HOD and Principal/Registrar with official seal as the case may be. The guides are responsible for timely submission of seminar paper, UC and SE.

11. If the guide wishes to leave the institution where the project is based, the Institute/Guide will inform the same to the Council and in consultation with Council, evolve steps to ensure successful completion of the project, before relieving the GUIDE.

12. Project proposals not in the prescribed format and incomplete will not be considered. **Advance copy and soft copy** of the proposals will not be considered.

13. Two copies of the proposal should be signed and forwarded by the Guide through HOD and Principal / Registrar as the case may be to reach the council office on or before **31 AUGUST 2019, 5.00 PM.**

14. Proposals received after the deadline will not be considered and no communication will be entertained in this regard. Postal delays will not be accepted on any ground.

-sd-

MEMBER SECRETARY

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FORMAT FOR STUDENT PROJECT PROPOSAL

1. Name of the Student (s) : S. Rahul, L. Sathish kumar, M. Santhosh kumar
   one valid e-mail id : rahulnaresh007@gmail.com.
2. Name of the Guide : T. KAMALKUMAR.
   Department / Designation : E.E.E/A.P.
   Institutional Address : TJS Engineering College, TJS Nagar, Peruvoyal.
   Phone No. & Mobile No. : 044-27967624 / 9843652109.
3. Project Title : AUTOMATIC FAULT DETECTION AND LOCATION OF TRANSI
   -ON LINE USING
4. Sector in which your Project proposal is to be Considered : **Agriculture/Biology/Physical/ Environment/ Medicine/ Veterinary/Social Sciences/Engineering& Tech.(Chemical /Computer Science/ Civil/ Mechanical/ Electrical, Electronics, Instrumentation, Communication) (Specify only one sector)**
5. Project Details : (write up (max. 5 pages only) is to be given for each item including justification for acquiring / fabricating equipments / apparatus in the budget)

   1. Introduction
   2. Objectives
   3. Methodology
   4. Work Plan
   5. Budget
   6. Any other details

7. Has a similar project been carried out in your college / elsewhere? If so furnish details of the previous project and highlight the improvements suggested in the present one : No.

CERTIFICATE

This is to certify that Mr./Miss. S. Rahul, L. Sathish kumar, M. Santhosh kumar. is a bonafide final year student of P.G. Science / U.G. Engineering / P.G. professional courses of our college and it is also certified that two copies of utilization certificate and final report along with seminar paper will be sent to the Council after completion of the project by the end of April 2020.

Signature of the Guide 31/8/19

Signature of the HOD 31/8/19

Signature of the Principal/ Head of the Institution 31-8-19

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N.B.: **2 copies of the proposals are to be submitted through proper channel to The Member Secretary, TNSCST, DOTE Campus, Chennai - 600 025 on or before 31 AUGUST 2019, 5 pm.**

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Automatic Fault Detection and Location of Transmission Lines using IoT

INTRODUCTION

Currently the electric power infrastructure is highly vulnerable against many forms of natural and malicious physical events which can adversely affect the overall performance and stability of the grid. Additionally, there is an impending need to equip the age-old transmission line infrastructure with a high-performance data communication network, that supports future operational requirements like real time monitoring and control necessary for smart grid integration

Wireless sensor-based monitoring of transmission lines provides a solution for several of these concerns like real time structural awareness, faster fault localization, accurate fault diagnosis by identification and differentiation of electrical faults from the mechanical faults, cost reduction due to condition based maintenance rather than periodic maintenance, etc.

These sensors can take fine grained measurements of a variety of physical or electrical parameters and generate a lot of information. Network design is a critical aspect of sensor-based transmission line monitoring due to the large scale, vast terrain, uncommon topology, and critical timing requirements. Mechanical faults, cost reduction due to condition-based maintenance rather than periodic maintenance, etc.

In Small-scale real-world deployments of wireless sensors include tension monitoring using load cells and power conductor surface temperature monitoring, sago meter, etc. This paper deals with the application of artificial neural networks (ANNs) to fault detection and location in extra high voltage (EHV) transmission lines for high speed protection using terminal line data by use of IOT

There are many courses of fault in power transmission power output, if not properly managed notable among them includes.

-fault at power generation station

-Damage to power transmission line

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ABSTRACT

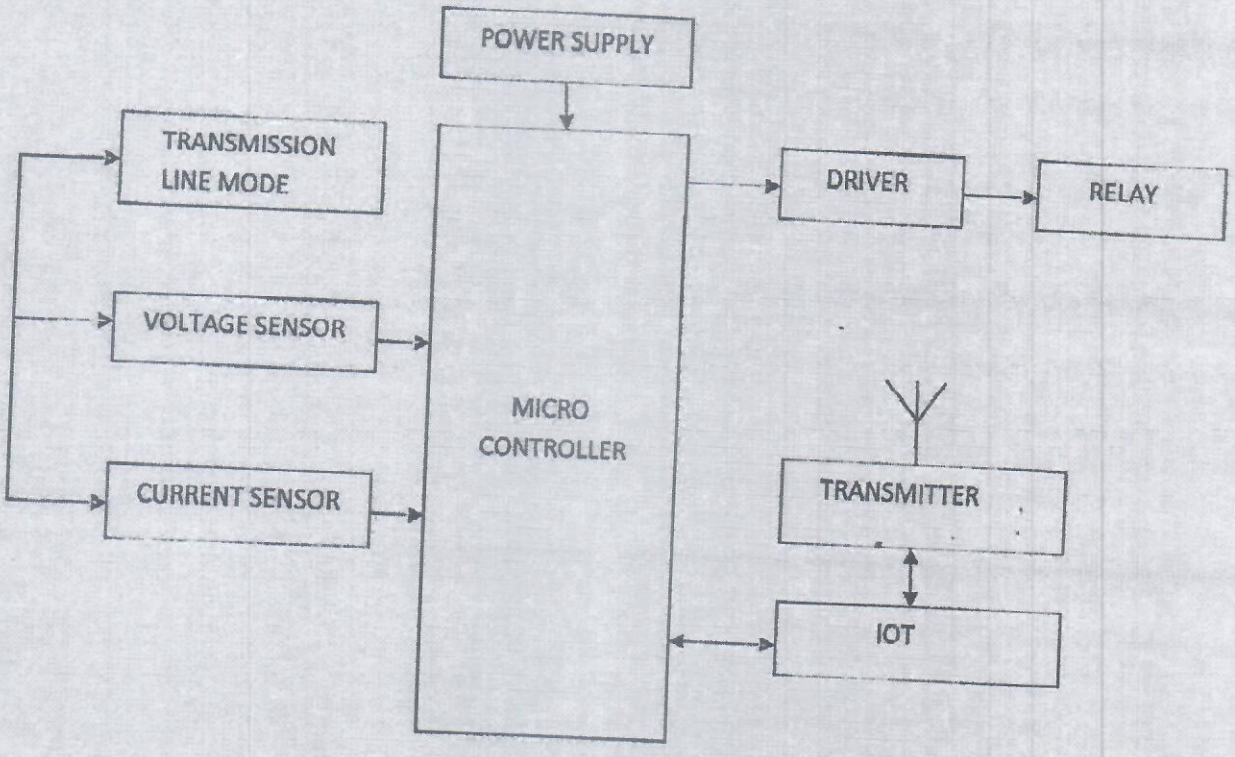
Energy leakage is one of the major problems that the corporation faces in recent times. Bringing this leakage under control is next to impossible with the electrical transmission lines running millions of miles across the country. Only way to solve this problem is to come up with a mechanism that can detect the fault in an electricity transmission line automatically and intimate the authorities with a specific location.

Through this project you will develop a device that uses sensors to sense the incoming & outgoing values and detect anomalies. And also the system will be integrated with the IoT mechanism, so as to intimate the responsible people real time with the location information and scale of leakage with an App.

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BLOCK DIAGRAM OF PROPOSED SYSTEM



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OBJECTIVE

In these project is mainly use to easily detect the fault and quickly protect the system and give information to main control center with the help of wireless sensors and communicate with IOT mechanism. In real time people easily find the location with the help of mobile app.

METHODOLOGY

1. PIC Microcontroller
2. IOT

WORK PLAN

S.NO	MONTH	WORK PLAN
01.	NOVEMBER	Theoretical analysis
02.	DECEMBER	Designing process of fault location tracker
03.	JANUARY	Collection of hardware components
04.	FEBRUARY	Arranging the setup , experimental verification and corrective measures
05.	MARCH	Project testing

BUDGET

S.NO	COMPONENTS	AMOUNT
01.	Micro controller unit	2500
02.	3 phase ratio transformer	700
03.	3 phase contractor	800
04.	Current sensor module	1200
05.	Voltage transformer module	1500
06.	IOT MODULE	800
07.	Transmitter & Receiver	650
08.	Relay & driver unit	400
09.	Fault location tracker	3000
10.	Hardware Testing	2500

TOTAL AMOUNT = 13300

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23/12/2020

From

Dr. R. Thenmozhi

HOD/EEE

TJSEC

To

The Principal,

TJSEC

Sir,

The following students of EEE Department had received a cash prize of Rs 7500/- from TNSCST under Student Project Scheme 2019-2020

Student Name	Guide Name.
1. S. Rahul	Mr. T. Kamal Kumar. AP/EEE
2. L. Sathish Kumar	
3. M. Santhosh Kumar.	

Hence the amount may be given to the students. I request you to be kind enough to do the needful so that the amount may be given as three individual cheques to the students for Rs 2500/.

Thank You.

Yours truly,

23/12/2020

Dr. R. Thenmozhi

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11/5/2020.

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தமிழ்நாடு அறிவியல் தொழில்நுட்ப மாநில மன்றம்
TAMILNADU STATE COUNCIL FOR SCIENCE AND TECHNOLOGY
(Established by Government of Tamilnadu)
Directorate of Technical Education Campus, Chennai – 600 025.
Ph : 044-22301428, Telefax : 044-22301552 www.tanscst.nic.in

Dr.R.SRINIVASAN, M.Sc., Ph.D.,F.I.C.S., M.A.C.S.(USA).,
Member Secretary

Lr.No.TNSCST/SPS/AR/2019-2020

20.03.2020

To
The Principal
T.J.S. Engineering College
Thiruvallur - 601 206

T.J.S. ENGINEERING COLLEGE
14 MAY 2020
PERUVOYAL, KAVARAIPETTAI-601 206.

Sir/Madam,

Sub: TNSCST – Student Project Scheme – 2019-2020 – approval intimation–grant release- reg.

With respect to the above scheme, the list of projects approved by the State Council is enclosed along with terms and conditions. You are requested to adhere to terms and conditions such as submission of UC and Seminar Paper in Time.

Herewith enclosed the cheque for the approved grant and disburse the grant to the concerned students through the guides at the earliest

Kindly send the utilisation certificate (format enclosed) and seminar paper (ref.T&C-no.5&6) on completion of the project.

Thanking you,

Yours faithfully,

20/5/20
Member Secretary.
20/5/20

Encl: a) Terms & Conditions (T&C)
b) Format of Utilisation Certificate (UC)
c) Cheque for Rs.7500/- No: 946115 dt.20.03.2020
Copy to: Individual Guides

HOD
EEE
18/5

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313. T.J.S. Engineering College (1) – 7500/-

	Mr. T. Kamalkumar Asst. Professor Dept. of EEE T.J.S. Engineering College Thiruvallur - 601 206	Automatic Fault Detection and Location of Transmission Lines using IoT	S. Rahul L. Sathish Kumar M. Santhosh Kumar	EEE-177	The Principal T.J.S. Engineering College Thiruvallur - 601 206	7500/-

OP 1815

EEE

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PAY The Principal, T.J.S. Engineering College, Thiruvallur. या धारक को OR BEARER

RUPEES रुपये Seven Thousand and five hundred only. अदा करें ₹ 7500/-

A/c. No. 4791.35159

[redacted]

VALID FOR THREE MONTHS ONLY
FROM THE DATE OF ISSUE W.E.F. 1.4.2012"

HMSFB
CBS CODE : 01636

Member Secretary
Tamilnadu State Council
for Science & Technology
Please Sign above

"946115" 600019119" 10

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AUTOMATIC FAULT DETECTION AND LOCATION OF TRANSMISSION LINES USING IOT

A PROJECT REPORT

Submitted by

RAHUL.S **(112816105009)**

SANTHOSH KUMAR.M **(112816105011)**

SATHISH KUMAR.L **(112816105901)**

In partial fulfilment for the award of the degree

Of

BACHELOR OF ENGINEERING

In

COMPUTER SCIENCE AND ENGINEERING

T.J.S. ENGINEERING COLLEGE, PERUVOYAL

ANNA UNIVERSITY: CHENNAI 600 025

APRIL 2020

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ANNA UNIVERSITY: CHENNAI 600 025

BONAFIDE CERTIFICATE

Certified that this project report "**AUTOMATIC FAULT DETECTION AND LOCATION OF TRANSMISSION LINE USING IOT**" is the bonafide work of the following students.

RAHUL.S	**(112816105009)**
SANTHOSH KUMAR.M	**(112816105011)**
SATHISH KUMAR.L	**(112816105901)**

Who carried out the project work under my supervision

SIGNATURE
Dr.R.THENMOZHI.,M.E.,Ph.D
HEAD OF THE DEPARTMENT
Department of Electrical and Electronics Engineering,
T.J.S. Engineering College,
Peruvoyal.

SIGNATURE
Mr.T.KAMALKUMAR.,M.E.,
SUPERVISOR
Department of Electrical and Electronics Engineering,
T.J.S. Engineering College,
Peruvoyal.

Submitted for viva voce held on 09.04.20 **at T.J.S. Engineering College, Peruvoyal.**

INTERNAL EXAMINER

T.J.S. ENGINEERING COLLEGE T.J.S.E.C. PERUVOYAL, KAVARAIPETTAI

EXTERNAL EXAMINER

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ACKNOWLEDGEMENT

"Project is the product out of experience that goes a long way in shaping up a person's calibre. The experience and success one attains is not by oneself but with a group of kind hearts behind."

First and foremost, we express our sincere thanks to honourable Founder and Chairman **"KALVI NERI KAVALAR" Shri. T.J.GOVINDARAJAN B.A.,** Managing Director & Secretary **Shri. T.J.ARUMUGAM.,** Vice Chairman **Shri. T.J.DESAMUTHU.,** Directors **Dr.A.PALANI B.D.S., Shri. A.VIJAYA KUMAR M.E., Shri. A.KABILAN BA. B.L., M.B.A., Shri. D.DINESH B.Com., L.L.B., Shri. G.TAMILARASAN B.Com.., M.B.A.,** for providing us with adequate infrastructure and congenital academic environment. We also record our sincere thanks to our honourable **Principal Dr. T.PALANI Ph.D.,** for his kind support to take up this project.

We express our gratitude to **Dr.R.THENMOZHI., Ph.D** Head of the Department of Electrical & Electronics Engineering whose guidance and encouragement has helped us in completing this project work.

We extend our sincere thanks to our guide **Mr.T..KAMALKUMAR M.E.,** and all other **TEACHING FACULTIES** and **NON-TEACHING STAFF** of Department of Electrical & Electronics Engineering for giving the confidence to complete the project successfully by providing the valuable suggestions and interest at every stage of the project.

Further the acknowledgement would be incomplete if we would not mention a word thanks to our most beloved **PARENTS** and **FRIENDS** whose continuous support and encouragement all the way through the course has led us to pursue the degree and confidently complete the project.

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ABSTRACT

Energy leakage is one of the major problems that the corporation faces in recent times. Bringing this leakage under control is next to impossible with the electrical transmission lines running millions of miles across the country. Only way to solve this problem is to come up with a mechanism that can detect the fault in an electricity transmission line automatically and intimate the authorities with a specific location. Through this project you will develop a device that uses sensors to sense the incoming & outgoing values and detect anomalies. And, the system will be integrated with the IoT mechanism, to intimate the responsible people real time with the location information and scale of leakage with an App.

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LIST OF ABBREVIATION

WI-FI	-	Wireless Fidelity
EEG	-	Electro Encephalography
BCI	-	Brain Computer Interface
CNN	-	Contingent Negative Variation
EXG	-	Electro Expectrogram
RAL	-	Robotics and Automation Laboratory
UART	-	Universal Asynchronous Receiver Transmitter
CMOS	-	Complementary Metal Oxide Semiconductor
TX	-	Transmit
RX	-	Receive
CISC	-	Complex Instruction Set
RISC	-	Reduced Instruction Set Computer
DC	-	Direct Current
LCD	-	Liquid Crystal Display
PWM	-	Pulse Width Modulation
PAN	-	Personal Area Network
IDE	-	Integrated Development Environment
PIC	-	Peripheral Interface Controller
IC	-	Integrated Circuit
RSIC	-	Reduced Instruction Set Computer
EPROM	-	Erasable Programmable Read-only Memory
CPU	-	Central Processing Unit
CU	-	Control Unit
PORT	-	Portable
A/D	-	Analog To Digital
PWM	-	Pulse Width Modulation

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CHAPTER 1

1.1 INTRODUCTION

Currently, the electric power infrastructure is highly vulnerable against many forms of natural and malicious physical events [1], which can adversely affect the overall performance and stability of the grid. Additionally, there is an impending need to equip the age-old transmission line infrastructure with a high-performance data communication network, that supports future operational requirements like real time monitoring and control necessary for smart grid integration [2], [3]. Many electric power transmission companies have primarily relied on circuit indicators to detect faulty sections of their transmission lines. However, there are still challenges in detecting the exact location of these faults. Although fault indicator technology has provided a reliable means to locate permanent faults, the technical crew and patrol teams still must physically patrol and inspect the devices for longer hours to detect faulty sections of their transmission lines. Wireless sensor-based monitoring of transmission lines provides a solution for several of these concerns like real time structural awareness, faster fault localization, accurate fault diagnosis by identification and differentiation of electrical faults from the mechanical faults, cost reduction due to condition based maintenance rather than periodic maintenance, etc. These applications specify stringent requirements such as fast delivery of enormous amount of highly reliable data. The success of these applications depends on the design of cost effective and reliable network architecture with a fast response time. The network must be able to transport sensitive data such as current state of the transmission line and control information to and from the transmission grid. This research provides a cost optimized framework to design a real time data transmission network. To monitor the status of the power system in real time,

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sensors are put in various components in the power network. These sensors can take fine grained measurements of a variety of physical or electrical parameters and generate a lot of information. Delivering this information to the control center in a cost efficient and timely manner is a critical challenge to be addressed in order to build an intelligent smart grid. Network design is a critical aspect of sensor-based transmission line monitoring due to the large scale, vast terrain, uncommon topology, and critical timing requirements. Mechanical faults, cost reduction due to condition-based maintenance rather than periodic maintenance, etc. The use of sensor networks has been proposed for several applications like mechanical state processing and dynamic transmission line rating applications [4]-[6]. To monitor the status of the power system in real time, sensors are put in various components in the power network [10]– [9]. The hierarchical model proposed in, offers a very expensive solution with the idea of deploying cellular transceivers on every tower. While such a network can provide extremely low latency data transmission, this model is highly cost inefficient as it incurs huge installation and subscription costs. The only work that addresses the problem of finding optimal locations of cellular transceivers is presented [11], [12]. The paper presents a digital fault locator by dynamic system parameter estimation for a double end fed transmission line. The authors of [13] and [14] were the first to propose a two-level model specifically for supporting the overhead transmission line monitoring applications. But considering the topological constraints posed by the transmission lines, the low band-width, low data rate wireless nodes would fail to transmit huge amount of data in a multi hop manner. In these works, the goal is to deploy multiple different sensors in critical and vulnerable locations of the transmission line to sense mechanical properties of its various components and transmit the sensed data through a suitable wireless network to the control center. However, most of these works address this theme at a very high level of abstraction. Small-scale real-world

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deployments of wireless sensors include tension monitoring using load cells [5]-[7], and power conductor surface temperature monitoring, sago meter, etc. This paper deals with the application of artificial neural networks (ANNs) to fault detection and location in extra high voltage (EHV) transmission lines for high speed protection using terminal line data. The proposed neural fault detector and locator were trained using various sets of data available from a selected power network model and simulating different fault scenarios (fault types, fault locations, fault resistances and fault inception angles) and different power system data (source capacities, source voltages, source angles, time constants of the sources) [8].

There are many courses of faults in power transmission leading to power outages, if not properly managed. Notable among them includes: – Faults at the power generation station – Damage to power transmission lines (tree falling on lines) – Faults at the substations or parts of distribution subsystem – Lightening Types of transmission line faults: Power system's faults may be categorized as shunt faults or series faults

1.2 AIM OF PROJECT

Over the past years, studies on monitoring the health of AECs used in DC/DC, AC/DC and DC/AC power converters have been reported. In DC/DC converters, these schemes utilize the information of capacitor voltage ripple and/or inductor current to estimate C and ESR of AEC. In single/three-phase AC/DC converters, condition monitoring schemes are presented mainly using modeling approaches or recursive algorithms. An external current/voltage signal is injected in the control loops with complex algorithms such recursive least square (RLS) and state vector machine (SVM), are used to estimate ESR and/or C. Several capacitor health monitoring methods in dc link capacitors in single-phase/three-phase

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DC/AC converters for solar and motor drive applications are presented in. However, research on the techniques for monitoring the health of SM capacitors used in an MMC is very limited. In, condition monitoring of SM capacitors based on RLS algorithm is introduced to estimate the capacitance. However, this approach requires the injection of an external CC in the control loop of the MMC to estimate capacitance, which further increases the capacitor voltage ripple and power losses. Moreover, the magnitude of external CC injection in the control loop is to be calculated either off-line or on-line, which complicates the controller design and signal injection. Kalman filter algorithm is employed for an MMC to estimate the capacitance of the SM capacitors. However, these approaches utilize the integral computation to estimate the SM capacitance of all capacitors in an arm, it would complicate the algorithm and increase the computational burden. The summary of aforementioned capacitor health monitoring schemes used in different power converters

1.3 SCOPE OF THE PROJECT

In this paper, a simple failure prediction technique for SM capacitors of an MMC is proposed by monitoring the second harmonic impedance utilizing the ripple in SM capacitor voltage and current. The proposed approach does not require any complicated algorithm and an external current/voltage signal injection in the control loop. Therefore, the proposed scheme offers easier implementation in digital controllers in comparison with the aforementioned approaches. The proposed scheme is validated by detailed simulation and experimental studies on a half-bridge sub module (HB-SM) based single-phase MMC (four SMs per arm). The presented results are in good agreement with the capacitance value measured using the LCR meter.

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CHAPTER 2

LITERATURE SURVEY

POWER SYSTEM CONNECTIVITY MONITORING USING A GRAPH THEORY NETWORK FLOW ALGORITHM

ABSTRACT:

A method of applying network flow analyses during real time power system operation, to provide better network connectivity visualization, is developed and presented. Graph theory network flow analysis is capable of determining the maximum flow that can be transported between two nodes within a directed graph.These network flow algorithms are applied to a graphical representation of a power system topology to determine the minimum number of system branches needed to be lost in order to guarantee disconnecting the two nodes in the system that are selected.The number of system branches that are found serves as an approximate indicator of system vulnerabilities. The method used in these connectivity analyses makes use of well known graph theory network flow maximum flow algorithms, but also introduces a new algorithm for updating an old network flow solution for the loss of only a single system branch.The proposed new algorithm allows for significantly decreased solution time that is desired in a real-time environment. The value of using the proposed method is illustrated by using a detailed example of the 2008 island formation that occurred in the 20,000-bus model of the Entergy system to show both the proposed method's benefits as well as practicality of implementation.

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AUTHORS: Trevor WerhoVijay VittalSharmaKolluri

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1. THE VALUE OF RECOVERY TRANSFORMERS IN PROTECTING AN ELECTRIC TRANSMISSION GRID AGAINST ATTACK

ABSTRACT:

This paper incorporates, as part of an attacker-defender (AD) model for an electric power transmission grid, an inventory of "recovery spares" for high-voltage transformers (HVTs).In this sequential-game model, an attacker first uses limited resources to disable grid components, seeking to maximize second-stage "total cost."This value corresponds to a defender who operates the damaged grid to minimize generating and economic load-shedding costs. The defender's problem includes 1) optimal power-flow solutions to represent post-attack operations, 2) optimized replacement of disabled HVTs with quickly installable recovery spares, and 3) longer-term replacements using new procurements. Global Benders decomposition, with a mixed-integer subproblem, solves the AD model; new enumerative techniques help solve the decomposition's master problem and subproblems.Computational tests demonstrate tradeoffs between the number of recovery spares and worst-case total cost, and show how the model could help guide an inventory strategy for recovery spares in an adversarial setting.

PUBLISHED IN: IEEE Transactions on Power Systems(Volume: 30, Issue: 5, Sept. 2015)

AUTHORS: Javier SalmeronR. Kevin Wood

3. BILEVEL PROGRAMMING APPLIED TO POWER SYSTEM VULNERABILITY ANALYSIS UNDER MULTIPLE CONTINGENCIES

ABSTRACT:

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This study examines the use of bilevel programming to analyse the vulnerability of power systems under multiple contingencies. One of the main purposes of this study is to explain the state of the art of the subject matter. A minimum vulnerability model and a maximum vulnerability model are presented and discussed.In both models, the upper-level optimisation determines a set of simultaneous outages in the transmission network whereas the lower-level optimisation models the reaction of the system operator against the outages identified in the upper level.The system operator reacts by minimising the system load shed through an optimal operation of the power system. Two solution approaches for the resulting mixed-integer non-linear bilevel programs are analysed and compared.Both methodologies are based on the equivalent transformation of the lower-level problem into a set of constraints, so that the original bilevel programs, respectively, become a single-level optimisation problem.The first approach is based on the application of Karush-Kuhn-Tucker optimality conditions whereas the second procedure relies on duality theory.This study shows that both approaches are essentially equivalent from a rigorous mathematical viewpoint; however, the second method is more suitable for off-the-shell branch-and-cut software as corroborated by numerical simulations.

PUBLISHED IN: IET Generation, Transmission & Distribution(Volume: 4, Issue: 2, February 2010)

AUTHORS: J.M. Arroyo Universidad de Castilla - La Mancha, Spain

4. CASCADING FAILURE ANALYSIS FOR INDIAN POWER GRID

ABSTRACT:

Major power grid blackouts in various parts of the world are characterized by voltage collapse. This paper studies the blackout case in theIndian power grid

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due to voltage collapse in the inter-regional corridor. First, the computer simulation models are tuned to match responses from the phasor measurement units at various locations in the grid.The inter-area mode with the frequency of 0.3 and 0.5 Hz with reduced damping were observed and resulted due to switching actions that occurred during the disturbance.This paper simulates the complex power grid network for various loading conditions of Northern region using power system simulator for engineering. Further, the system variables are analyzed using Prony method to estimate the inter-area mode for different NR loading conditions.Theeigen values associated with the 0.3 Hz mode depict the movement from open left half plane into open right half plane with a slight increase in the parameter indicating "hopfbifurcation."This paper also discusses the maximum loading capacity for the inter-regional lines in-order avoid loss of small signal stability, and highlights the use of real time phasor measurement unit measurements in-order to estimate and track the oscillatory modes.

PUBLISHED IN: IEEE Transactions on Smart Grid(Volume: 7, Issue: 4, July 2016)

AUTHORS: VaishaliRampurkar PolganiPentayya Harivittal A. Mangalvedekar

5. CAUSES OF THE 2003 MAJOR GRID BLACKOUTS IN NORTH AMERICA AND EUROPE, AND RECOMMENDED MEANS TO IMPROVE SYSTEM DYNAMIC PERFORMANCE

ABSTRACT:

On August 14, 2003, a cascading outage of transmission and generation facilities in the North American Eastern Interconnection resulted in a blackout of

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most of New York state as well as parts of Pennsylvania, Ohio, Michigan, and Ontario, Canada.

On September 23, 2003, nearly four million customers lost power in eastern Denmark and southern Sweden following a cascading outage that struck Scandinavia. Days later, a cascading outage between Italy and the rest of central Europe left most of Italy in darkness on September 28.These major blackouts are among the worst power system failures in the last few decades. The Power System Stability and Power System Stability Controls Subcommittees of the IEEE PES Power System Dynamic Performance Committee sponsored an all day panel session with experts from around the world.The experts described their recent work on the investigation of grid blackouts. The session offered a unique forum for discussion of possible root causes and necessary steps to reduce the risk of blackouts.This white paper presents the major conclusions drawn from the presentations and ensuing discussions during the all day session, focusing on the root causes of grid blackouts.This paper presents general conclusions drawn by this Committee together with recommendations based on lessons learned.

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AUTHORS: G. Andersson P. Donalek R. Farmer

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CHAPTER 3

EXISTING AND PROPOSED SYSTEM

3.1 EXISTING SYSTEM

- In the existing process there is no automatic system for finding the power line break occurrence.
- Until now human needs is the only solution for finding those problems.
- To overcome this we are going to deal with the new techniques.

3.1.1 Block Diagram Of Existing System

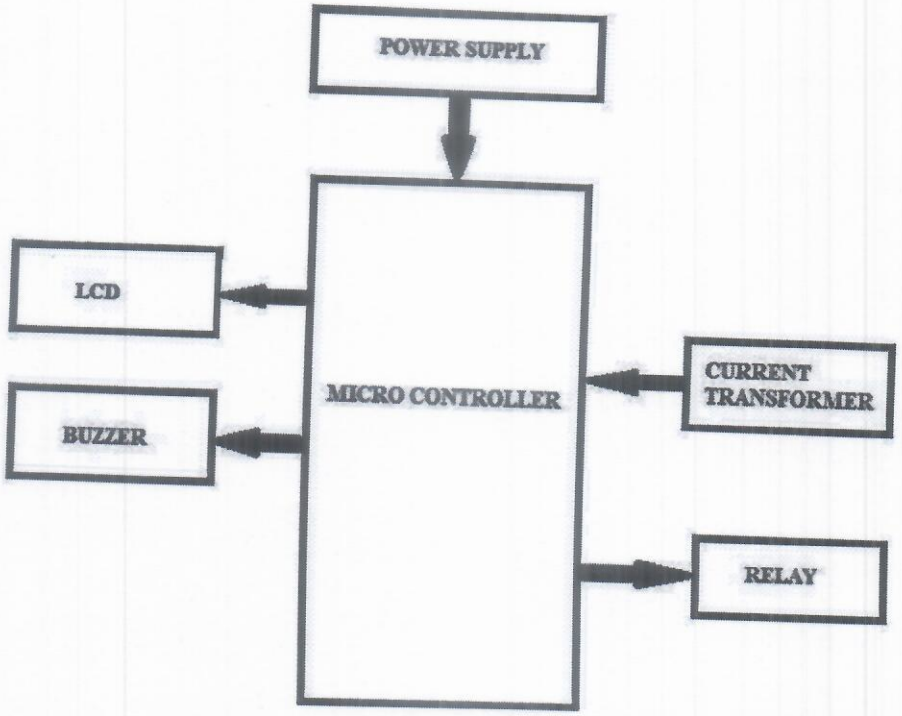


Fig.No.3.1 Block Diagram Of Existing System

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3.2 The Proposed System

In this proposed system we are continuously monitoring the power line disconnection due to any physical breakage in the cables. The first section consists of a voltage regulator. The voltage regulator is used to measure the input voltage from the power station and that value is transmitted to the next section using WSN.The driver circuit is used to control the voltage from power station to the next section.The next section receives the voltage level from first section and measures the input voltage from the first section.If both values are approximately same, then it transmits the voltage to the next section.If a rapid change is found by the voltage regulator in the second section, then a signal is transmitted to the first section indicating that a rapid voltage change is occurred. And also the power supply from first section to second section is cut-off.

3.2.1 Block Diagram Of Proposed System

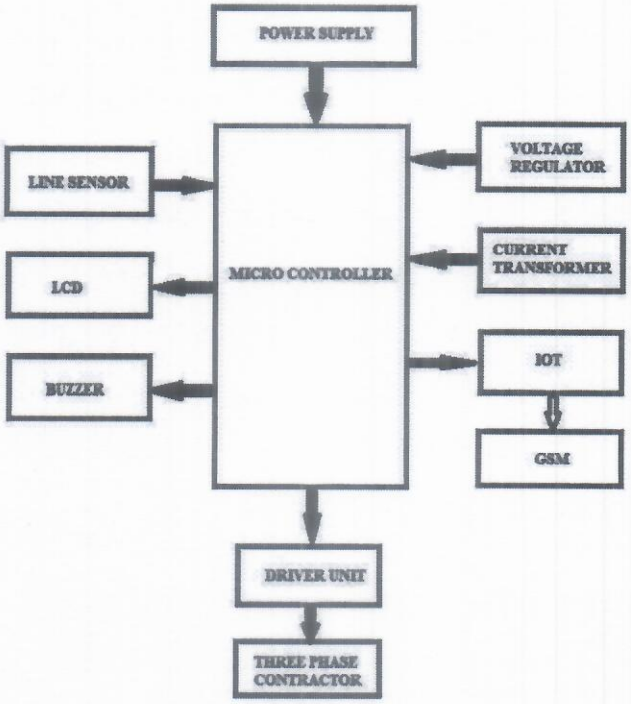


Fig.No.3.2 Block Diagram Of Proposed System

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CHAPTER 4

HARDWARE IMPLIMENTATION

DESCRIPTION OF HARDWARD REQUIREMENTS

4.1 POWER SUPPLY

4.1.1. Transformer

The potential transformer will step down the power supply voltage (0-230V) to (0-6V) level. Then the secondary of the potential transformer will be connected to the precision rectifier, which is constructed with the help of op-amp. The advantages of using precision rectifier are it will give peak voltage output as DC, rest of the circuits will give only RMS output.

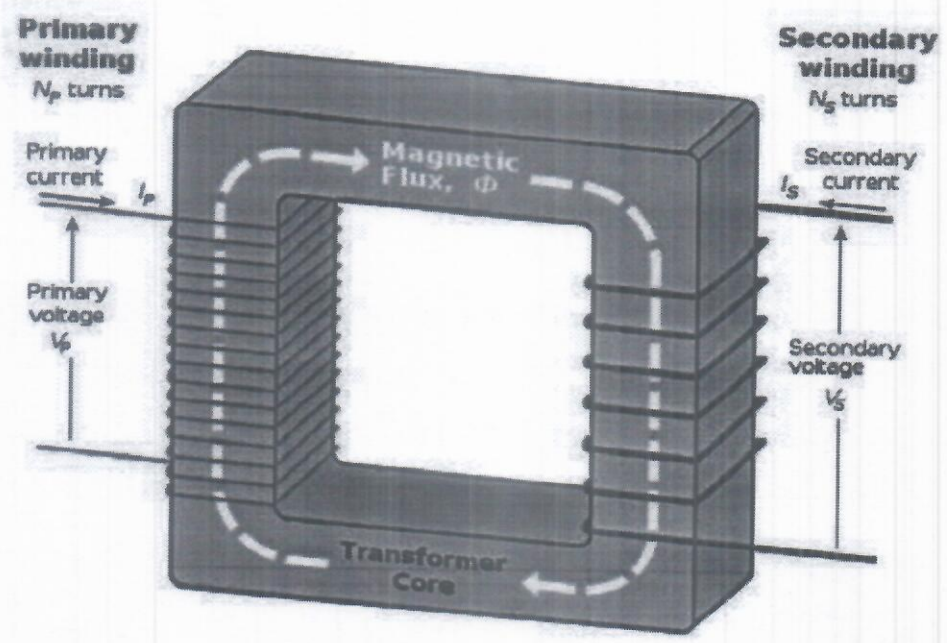


Fig.No.4.1 Potential Transformer

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4.1.2 Bridge Rectifier

When four diodes are connected as shown in figure, the circuit is called as bridge rectifier. The input to the circuit is applied to the diagonally opposite corners of the network, and the output is taken from the remaining two corners. Let us assume that the transformer is working properly and there is a positive potential, at point A and a negative potential at point B. the positive potential at point A will forward bias D3 and reverse bias D4.

The negative potential at point B will forward bias D1 and reverse D2. At this time D3 and DI are forward biased and will allow current flow to pass through them; D4 and D2 are reverse biased and will block current flow.

The path for current flow is from point B through DI, up through RL. through D3, through the secondary of the transformer back to point B. this path is indicated by the solid arrows. Waveforms (1) and (2) can be observed across DI and D3.

One-half cycle later the polarity across the secondary of the transformer reverse. forward biasing D2 and D4 and reverse biasing DI and D3.Current flow will now be from point A through D4, up through RL, through D2, through the secondary of T1, and back to point A. This path is indicated by the broken arrows. Waveforms (3) and (4) can be observed across D2 and D4. The current flow through RL is always in the same direction. In flowing through RL this current develops a voltage corresponding to that shown waveform (5). Since current flows through the load (RL) during both half cycles of the applied voltage, this bridge rectifier is a full-wave rectifier.

One advantage of a bridge rectifier over a conventional full-wave rectifier is that with a given transformer the bridge rectifier produces a voltage output that is nearly twice that of the conventional full-wave circuit.

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4.1.3 IC Voltage Regulators

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings. A fixed three-terminal voltage regulator has an unregulated de input voltage, Vi, applied to one input terminal, a regulated de output voltage, Vo, from a second terminal, with the third terminal connected to ground. The series 78 regulators provide fixed positive regulated voltages from 5 to 24 volts. Similarly, the series 79 regulators provide fixed negative regulated voltages from 5 to 24 volts.

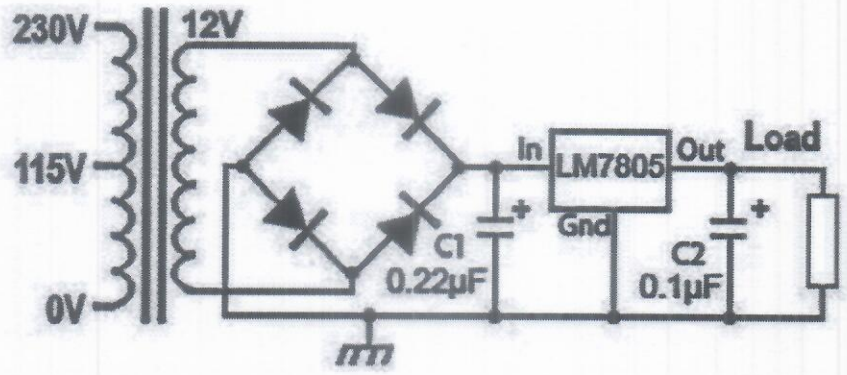


Fig.No.4.2 IC Voltage Regulators

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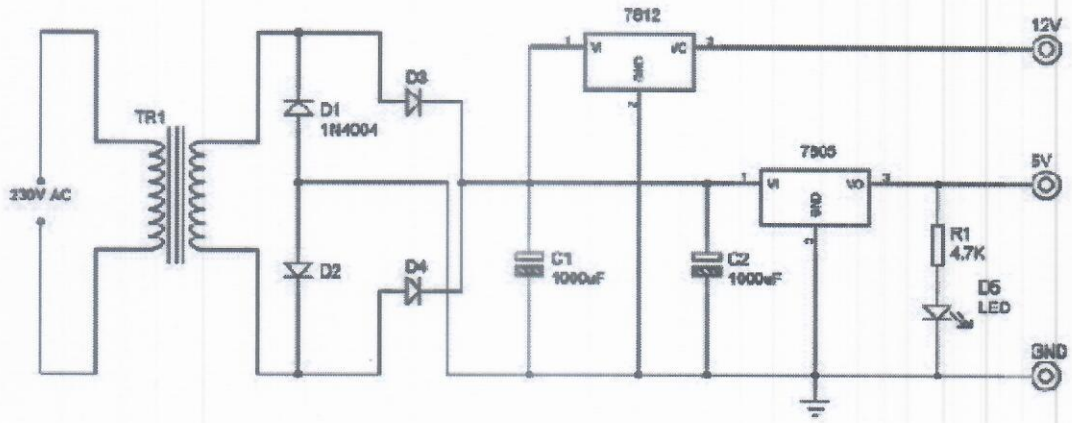


Fig.No.4.2.1 IC Voltage Regulators

4.2 Microcontroller

4.2.1 Introduction

All the functions required on a single chip. A microcontroller differs from a microprocessor, which is a general-purpose chip that is used to create a multi-function computer or device and requires multiple chips to handle various tasks. A microcontroller is meant to be more self contained and independent, and functions as a tiny, dedicated computer. They are typically designed using CMOS (complementary metal oxide semiconductor) technology, an efficient fabrication technique that uses less power and is more immune to power spikes than other techniques. There are also multiple architectures A microcontroller is an integrated chip that is often part of an embedded system.

The microcontroller includes a CPU, RAM, ROM, LO ports, and timers like a standard computer, but because they are designed to execute only a single specific task to control a single system, they are much smaller and simplified so that they can include used, but the predominant architecture is CISC (Complex Instruction Set Computer), which allows the microcontroller to contain multiple

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control instructions that can be executed with a single macro instruction. Some use a RISC (Reduced Instruction Set Computer) architecture, which implements fewer instructions, but delivers greater simplicity and lower power consumption.

Early controllers were typically built from logic components and were usually quite large. Later, microprocessors were used, and controllers were able to fit onto a circuit board. Microcontrollers now place all of the needed components onto a single chip. Because they control a single function, some complex devices contain multiple microprocessors.

Microcontrollers have become common in many areas, and can be found in home appliances, computer equipment, and instrumentation. They are often used in automobiles, and have many industrial uses as well, and have become a central part of industrial robotics. Because they are usually used to control a single process and execute simple instructions, microcontrollers do not require significant processing power. Products like CD players, hi-fi equipment, video games, washing machines, cookers and so on fit into this category. The communications market, automotive market, and the military share the rest of the application areas. Microcontrollers have traditionally been programmed using the assembly language of the target microcontroller. Different microcontrollers from different manufacturers have different assembly languages.

Assembly language consists of short mnemonic descriptions of the instruction sets. These mnemonics are difficult to remember and the programs developed for one microcontroller cannot be used for other types of microcontrollers. The most common complaint about microcontroller programming is that the assembly language is somewhat difficult to work with, especially during the development of complex projects.

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The solution to this problem is to use high-level languages. This makes the programming a much simpler task and the programs are usually more readable, portable, and easier to maintain. There are various forms of BASIC and C compilers available for most microcontrollers. BASIC compilers are usually in the form of interpreters and the code produced is usually slow.

4.2.2 Evolution Of Microcontroller

First, microcontrollers were developed in the mid-1970s. These were basically calculator-based processors with small ROM program memories, very limited RAM data memories, and a handful of input/output ports. As silicon technology developed, more powerful, 8-bit microcontrollers were produced. In addition to their improved instruction sets, these microcontrollers included on-chip counter/timers, interrupt facilities, and improved LO handling. On-chip memory capacity was still small and was not adequate for many applications. One of the most significant developments at this time was the availability of on-chip ultraviolet erasable EPROM memory. This simplified the product development time considerably and, for the first time, also allowed the use of microcontrollers in low-volume applications.

4.2.3 Introduction Of 8051 Family

The 8051 family was introduced in the early 1980s by Intel. Since its introduction, the 8051 has been one of the most popular microcontrollers and has been second-sourced by many manufacturers. The 8051 currently has many different versions and some types include on-chip analogue-to-digital converters, a considerably large size of program and data memories, pulse- width modulation on outputs, and flash memories that can be erased and reprogrammed by electrical signals. Microcontrollers have now moved into the 16-bit market. 16-bit micro-controllers are high-performance processors that and applications in real-time and

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compute intensive fields (e.g. in digital signal processing or real-time control). Some of the 16-bit microcontrollers include large amounts of program and data memories, multi-channel analogue-to-digital converters, a large number of 1/O ports, several serial ports, high-speed arithmetic and logic operations, and a powerful instruction set with signal processing capabilities. The simplest microcontroller architecture consists of a microprocessor, memory, and input/output. The microprocessor consists of a central processing unit (CPU) and the control unit (CU).The CPU is the brain of a microprocessor and is where all of the arithmetic and logical operations are performed. The control unit controls the internal operations of the microprocessor and sends control signals to other parts of the microprocessor to carry out the required instructions. Memory is an important part of a microcomputer system. Depending upon the application we can classify memories into two groups: program memory and data memory. Program memory stores all the program code. This memory is usually a read-only memory (ROM). Other types of memories, e.g. EPROM and PEROM flash memories are used for low-volume applications and also during program to that development. Data memory is a read/write memory (RAM).In complex applications where there may be need for large amounts of memory it is possible to interface external memory chips to most microcontrollers. Input/ Output (/0) ports allow external digital signals to be connected to the microcontroller. I/O ports are usually organized into groups of 8 bits and each group is given a name. For example, the 8051 microcontroller contains four8- bit I/O ports named PO, PI, P2, and P3. On some microcontrollers the direction of the 1/O port lines are programmable so that different bits of a port can be programmed as inputs or outputs. Some microcontrollers (including the8051 family) provide bi-directional 1/O ports. This basic device is now available in several configurations. Each 1/O port line of such microcontrollers can be used as inputs and outputs. Some microcontrollers provide

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'open-drain' outputs where the output transistors are left floating (e.g. port P0 of the 8051 family). External pull-up resistors are normally used with such output port lines.

4.2.4 8051 Family

The 8051 family is a popular, industry standard 8-bit single chip micro-computer (microcontroller) family, manufactured by various companies with many different capabilities. The basic standard device, which is the first member of the family, is the 8051, which is a 40-pin microcontroller. This basic device is now available in several configurations. The 80C51 is the low-power CMOS version of the family. The 8751 contains EPROM program memory, used mainly during development work. The 89C51 contains flash programmable and erasable memory (PEROM) where the program memory can be reprogrammed without erasing the chip with ultraviolet light. The 8052 is an enhanced member of the family which contains more RAM and also more timer/counters. There are many versions of the 40-pin family which contain on-chip analogue-to-digital converters, pulse-width modulators, and so on. At the lower end of the 8051 family we have the 20-pin microcontrollers which are code compatible with the 40-pin devices. The 20-pin devices have been manufactured for less complex applications where the 1/O requirements are not very high and where less power is required (c.g. in portable applications). The AT89C1051 and AT89C2051 (manufactured by Atmel) are such microcontrollers, which are fully code compatible with the 8051 family and offer reduced power and less functionality. The 8051 is an 8-bit, low-power, high-performance microcontroller. There are a large number of devices in the 8051 family with similar architecture and each member of the family is downward compatible with each other. The basic 8051microcontroller has the following features: 4 Kbytes of program memory

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- 256*8 RAM data memory
- 32 programmable 1/O lines
- Two 16-bit timer/counters
- Six interrupt sources
- External memory interface
- Standard 40-pin package

4.3 Pic Microcontroller

The PIC microcontroller PIC16(877A is one of the most renowned microcontrollers in the industry. This controller is very convenient to use, the coding or programming of this controller is also easier. One of the main advantages is that it can be write-erase as many times as possible because it use FLASH memory technology. It has a total number of 40 pins and there are 33 pins for input and output. PIC16F877A is used in many PIC Microcontroller projects. PICI 6F877A also have many applications in digital electronics circuits.

4.3.1 PIC16F877A

The term PIC, or Peripheral Interface Controller, is the name given by Microchip Technologies to its single- chip microcontrollers. PIC micros have grown to become the most widely used microcontrollers in the 8- bit microcontroller segment. The PIC16F877A CMOS FLASH-based 8-bit microcontroller is upward compatible with the PIC16C5X, PIC12CXXX and PIC16C7x devices. It features 200 ns instruction execution, 256 bytes of EEPROM data memory, self-programming, an ICD, 2 Comparators, 8 channels of 10-bit Analog-to-Digital (A/D) converter, 2 capture/compare/PWM functions, a synchronous serial port that can be configured as either 3-wire SPI or 2-wire 12C bus, a USART, and a Parallel Slave Port.

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4.3.2 Special Microcontroller Features

- Flash Memory: 14.3 Kbytes (8192 words)
- Data SRAM: 368 bytes
- Data FEPROM: 256 bytes
- Self-reprogrammable under software control
- In circuit serial programming via two pins (5V)
- Watchdog Timer with on-chip RC oscillator
- Programmable code protection
- Power-saving Sleep mode
- In-Circuit Debug via two pins
- 10-bit, 8-channel A/D Converter
- Brown-Out Reset
- Analogue Comparator module

4.3.3 Peripheral Features

- 33 1/O pins; 5 1/O ports
- Timer 0: 8-bit timer/counter with 8-bit pre scalar
- Timer 1: 16-bit timer/counter with pre scalar
- Can be incremented during Sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, pre scalar and pos scalar
- Two Capture, Compare, PWM modules
- 16-bit Capture input; max resolution 12.5 ns
- 16-bit Compare; max resolution 200 ns
- 10-bit PWM

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- Synchronous Serial Port with two modes:
- SPI Master
- 12C Master and Slave
- USART/SCI with 9-bit address detection
- Parallel Slave Port (PSP)
- 8 bits wide with external RD, WR and CS controls
- Brown-out detection circuitry for Brown-Out Reset

The internal block diagram of PIC16F877 is shown in the figure. It contains 4-banks of register files such as Bank 0, Bank 1, Bank 2 and Bank 3 from 00h- 07h, 80h-FFh, 100h-17FH and 180h-1FFH respectively. And it is also having program FLASH memory, Data memory and Data EEPROM of 8K, 368 and 256 Bytes respectively.

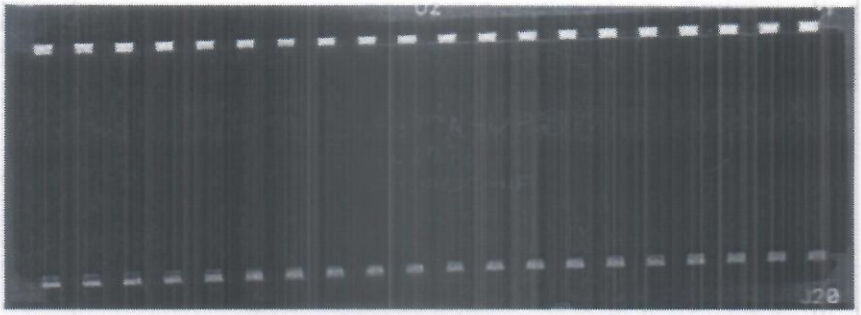


Fig.No.4.3 PIC16F877A

4.3.4 Register File

The term register file in PIC terminology used to denote the locations than an instruction can access via an address. The register file consists of two components, they are

- General purpose register file
- Special purpose register file

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4.3.5 General Purpose Register File

The general-purpose register file is another name for the microcontrollers RAM. Data can be written to each 8-bit location, updated and retrieved any number of times. All control registers are coming under the general purpose register file.

4.3.6 Special Purpose Register File

The special purpose register file contains input and output ports as well as the control registers used to establish each bit of port as either an input or output. It contains registers that provide the data input and data output to the variety of resources on the chip, such as the timers, the serial ports and the analogy-to-digital converter.

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Architecture of PIC16F877A

Device	Program FLASH	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes

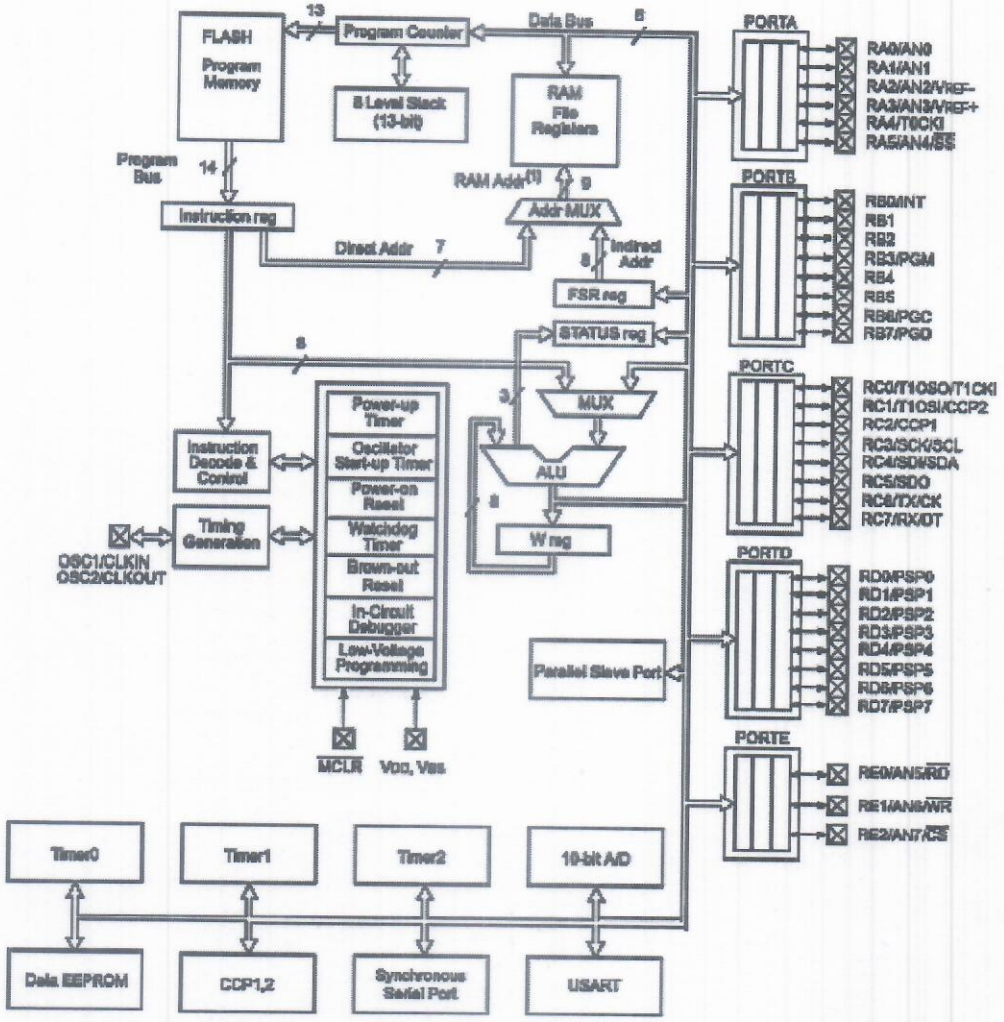


Fig.No.4.4 Architecture of PIC16F877A

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4.3.7 Pin Description

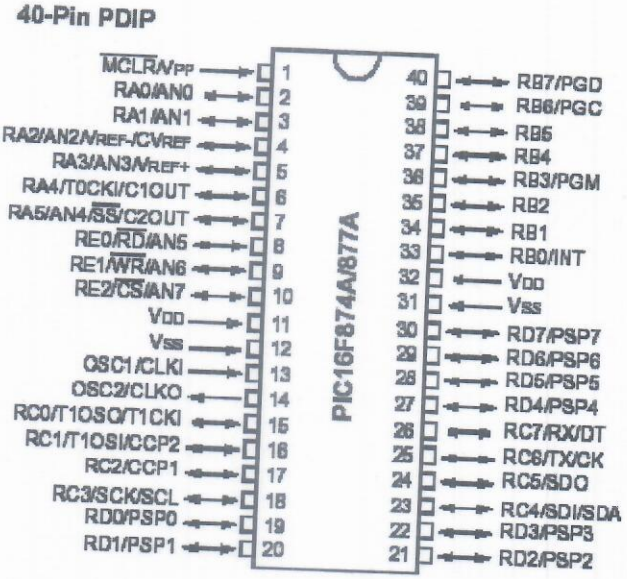


Fig.No.4.5 Pin Diagram of PIC16F877A

The pins RBO-RB7, RC0-RC7, and RD0-RD7 are digital I/O pins. The pins CCPI and CCP2, which share locations with RCI and RC2, can be used for a PWM signal (see DC Motor tutorial). The pins AN0-AN7 are for analog 1/O (see Photo resistor tutorial). TX and RX are for debugging 1/O (see Output Messages to Computer tutorial). The remaining pins deal with power/ground, the clock signal, and programmer 1/O.

A PIC is made of several "ports." Each port is designated with a letter, RB0-RB7 are a port. RC0-RC7 and RD0-RD7 are a port as well. RA0-RA5 and RE0-RE2 are also ports, but with fewer pins. Some of these pins have special purposes, but most can be used as basic input/output pins.

For example, you can set pin RB0 to be either an input pin, or an output pin. As an input pin, the digital voltage on the pin can be read in. For example, if RBO

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is connected to ground (0v), then you would read a digital 0. If RB0 was connected to power (5v), then you would read a digital 1.

4.3.8 Memory Organization

There are three memory blocks in each of the PIC16F87XA devices. The Program Memory and Data Memory have separate buses so that concurrent access.

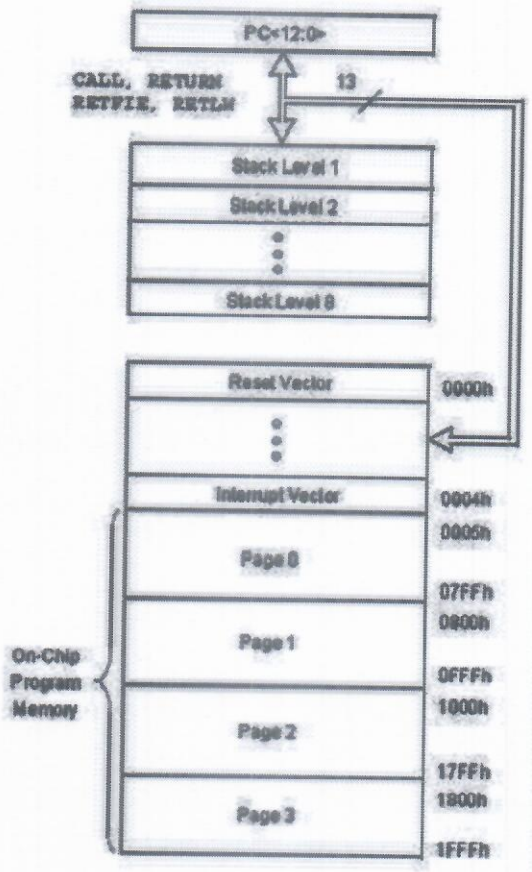


Fig.No.4.6 Memory Organization Of PIC168877

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4.3.9 Program Memory Organization

The PIC16F87XA devices have a 13-bit program counter capable of addressing an 8K word. The PIC16F876A/877A devices have 8K words x 14 bits of FLASH program bit program memory space. memory, while PIC16F873A/874A devices have 4K words x 14 bits. Accessing a location above the physically implemented address will cause a wraparound. The RESET vector is at 0000h and the interrupt vector is at 0004h.

4.3.10 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RPI (STATUS<6>) and RPO (STATUS<5>) are the bank select bits.

RP1:RP0	BANK
00	0
01	1
10	2
11	3

Table.No.4.1 Register and Bank Allocation

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some of these pins have special purposes, but most can be used as basic input/output pins. Some frequently

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used Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

4.3.11 Master Mode

Master mode of operation is supported by interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a reset or when the MSSP module is disabled. In master mode, the SCL and SDA lines are manipulated by the MSSP hardware. The following events will cause the SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received
- Acknowledge transmit
- Repeated Start

4.3.12 Analog-To-Digital Converter (A/D) Module

The analog input charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation.

The A/D conversion of the analog input signal results in a corresponding 10-bit digital number. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)

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• A/D Result Low Register (ADRESL)

• A/D Control Register0 (ADCON0)

• A/D Control Register1 (ADCON1)

The ADCON0 register, controls the operation of the A/D module. The ADCON1 register, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference) or as digital I/O.

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set.

The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:

• Configure analog pins / voltage reference / and digital I/O (ADCON1)

• Select A/D input channel (ADCON0)

• Select A/D conversion clock (ADCON0)

• Turn on A/D module (ADCON0)

2. Configure A/D interrupt (if desired):

• Clear the ADIF bit

• Set the ADIE bit

• Set the GIE bit

3. Wait the required acquisition time.

4. Start conversion:

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• Set the GO/DONE bit (ADCON0)

5. Wait for A/D conversion to complete, by either:

• Polling for the GO/DONE bit to be cleared

OR

• Waiting for the A/D interrupt

6. Read A/D Result register (ADRES), clear the ADIF bit, if required.

7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is

defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

Acquisition time is the time that the A/D module's holding capacitor is connected to the external voltage level. Then there is the conversion time of 10 TAD, which is started when the GO bit is set. The sum of these two times is the sampling time. There is a minimum acquisition time to ensure that the holding capacitor is charged to a level that will give the desired accuracy for the A/D conversion.

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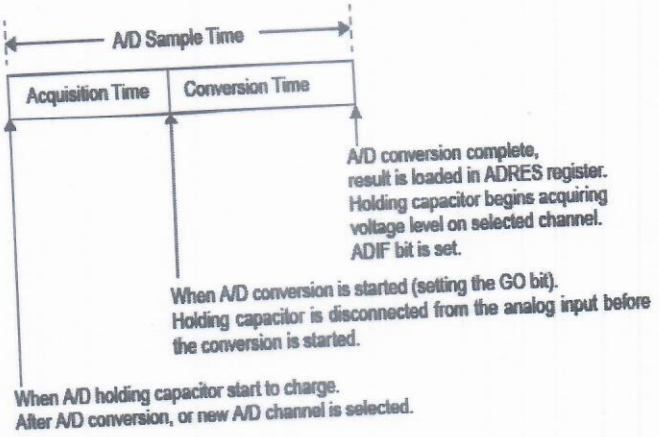


Fig.No. 4.7 Analog-To-Digital Converter (A/D) Module

4.3.13 Reset

The PIC16F87X differentiates between various kinds of reset:

- Power-on Reset (POR)
- MCLR reset during normal operation
- MCLR reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)
- Brown-out Reset (BOR)

Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on the MCLR and WDT Reset, on MCLR reset during SLEEP, and Brownout Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation.

A simplified block diagram of the on-chip reset circuit is shown in Fig 3.2.14. These devices have a MCLR noise filter in the MCLR reset path. The filter

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will detect and ignore small pulses. It should be noted that a WDT Reset does not drive MCLR pin low.

4.3.14 Interrupt

The PIC16F87X family has up to 14 sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits. A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if leared) all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set regardless of the status of the GIE bit. The GIE bit is cleared on reset. The "return from interrupt" instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables interrupts.

4.3.15 Int Intrrupt

External interrupt on the RB0/INT pin is edge triggered, either rising, if bit INTEDG (OPTION_REG<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP.

4.3.16 TMR0 Intrrupt

An overflow (FFh ® 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>).

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4.3.17 Port B Intcon Change

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/ disabled by setting/clearing enable bit RBIE (INTCON<4>).

4.4 Crystal Oscillator

4.4.1 General Description

A crystal oscillator is an electronic circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. This frequency is commonly used to keep track of time (as in quartz wristwatches), to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters/receivers

4.4.2 Product Description

Crystal Oscillators are usually, fixed frequency oscillators where stability and accuracy are the primary considerations. For example it is almost impossible to design a stable and accurate LC oscillator for the upper HF and higher frequencies without resorting to some sort of crystal control. Hence the reason for crystal oscillators. The crystal oscillator circuit usually works on the principle of the inverse piezoelectric effect. The applied electric field will produce a mechanical deformation across some materials. Thus, it utilizes the vibrating crystal's mechanical resonance, which is made with a piezoelectric material for generating an electrical signal of a particular frequency. Usually, quartz crystal oscillators are highly stable, consist of good quality factor(Q), they are small in size, and are economically related. Hence, quartz crystal oscillator circuits are more superior compared to other resonators like LC circuits, tuning forks. Generally in Microprocessors and Micro controllers we are using an 8MHz crystal oscillator.

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Fig. No.4.8 Crystal Oscillation

4.4.3 A Pratical Example for Crystal Oscillator

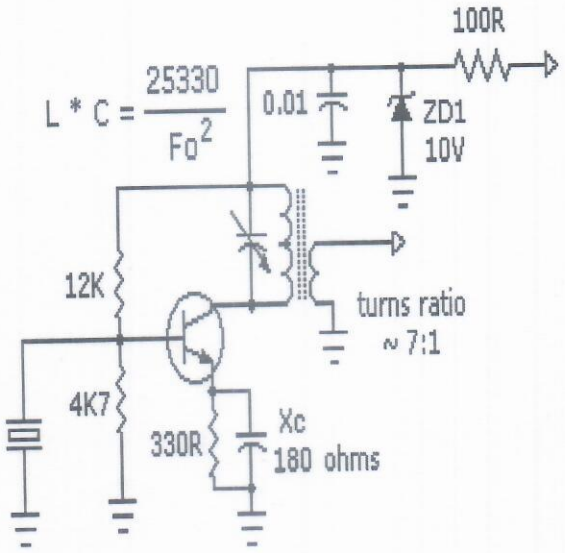


Fig.No. 4.9 A Pratical Example for Crystal Oscillator

This is a typical example of the type of crystal oscillators which may be used for say converters. Some points of interest on crystal oscillators.

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4.4.4 Oscillator Type

The PIC16F87XA can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low-Power Crystal
- XT Crystal/Resonator
- HS High-Speed Crystal/Resonator
- RC Resistor/Capacitor

4.4.5 Crystal Oscilllator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKI and OSC2/CLKO pins to establish oscillation. The Microcontroller oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications. When in XT, LP or HS modes, the device can have an external
clock source to drive the OSC1/CLKI pin.

4.4.6 RC Oscillator

For timing insensitive applications, the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure shows how the R/C combination is connected to the Microcontroller.

Notes:

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1: Higher capacitance increases the stability of oscillator but also increases the start-up time.

2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

3: ***Rs*** may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.

4: When migrating from other microcontroller devices, oscillator performance should be verified.

4.5 TLP 250 Driver

TLP250 is an isolated IGBT/Mosfet driver IC. The input side consists of a GaAlAs light-emitting diode. The output side gets a drive signal through an integrated photodetector. Therefore, the main feature is electrical isolation between low and high power circuits. It transfers electrical signals optically via light. Users can use it to drive gate terminal of high voltage switches in both configurations such as high side and low side drive. It is available as an 8-pin DIP package.

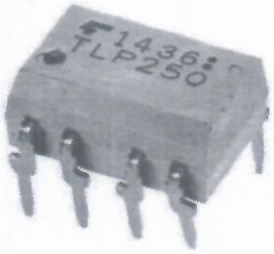


Fig.No.4.10 TLP 250 Driver

The Pinout diagram of TLP250 is given below. It is clearly shown in the figure that led at the input stage and photodetector diode at the output stage is used to provide isolation between high and low power circuits. Pin number 1 and 4 are not connected to any point. They are marked as NC (No connection). Hence they are not in use. Pin 2 is the anode point of input stage light emitting diode and pin 3

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is the cathode point of the input stage. Input is provided to pin number 2 and 3. Pin number 8 is for supply connection. Pin number 5 is for a ground of power supply.

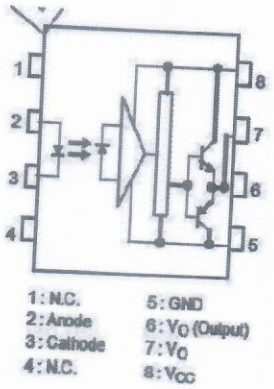


Fig.No.4.11 Pin Out of Driver

4.6 Current Transformer

The **Current Transformer (C.T.)**, is a type of "instrument transformer" that is designed to produce an alternating current in its secondary winding which is proportional to the current being measured in its primary. *Current transformers* reduce high voltage currents to a much lower value and provide a convenient way of safely monitoring the actual electrical current flowing in an AC transmission line using a standard ammeter. The principal of operation of a basic current transformer is slightly different from that of an ordinary voltage transformer.

Unlike the voltage or power transformer looked at previously, the current transformer consists of only one or very few turns as its primary winding. This primary winding can be of either a single flat turn, a coil of heavy duty wire wrapped around the core or just a conductor or bus bar placed through a central hole as shown.

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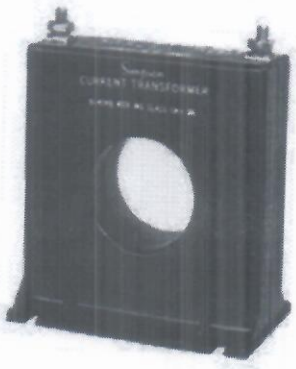


Fig.4.12 Typical Current Transformer

Due to this type of arrangement, the current transformer is often referred too as a "series transformer" as the primary winding, which never has more than a very few turns, is in series with the current carrying conductor supplying a load.

The secondary winding however, may have a large number of coil turns wound on a laminated core of low-loss magnetic material. This core has a large cross-sectional area so that the magnetic flux density created is low using much smaller cross-sectional area wire, depending upon how much the current must be stepped down as it tries to output a constant current, independent of the connected load.

The secondary winding will supply a current into either a short circuit, in the form of an ammeter, or into a resistive load until the voltage induced in the secondary is big enough to saturate the core or cause failure from excessive voltage breakdown.

Unlike a voltage transformer, the primary current of a current transformer is not dependent of the secondary load current but instead is controlled by an external load. The secondary current is usually rated at a standard 1 Ampere or 5 Amperes for larger primary current ratings.

4.7 Line Sensor

Line sensors are used for sensing white line on dark surface or black line on light surface. This line sensor board has three line sensors connected together. These sensors working together can follow any curved or zig-zag path. Because of

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multiple sensors it can even detect nodes and move on the maze of white or black lines. Line sensor consists of high intensity red LED for illumination and directional photo transistor for line sensing. Phototransistor consists of a photo transistor and convex lense. Because of precise alignment between lense and photo transistor it has very narrow viewing angle of 5 degrees. This makes this line sensor highly immune to ambient light. This sensor gives 0.18 volts on bright surface and gives 2.2V or more on the dark surface. Its output is analog in nature. Because of analog output one can write complex algorithm to follow white line using microcontroller. This sensor has very proven track record in various robotics competitions.

Specifications

- Supply: 5V, 60mA
- Sensor output: Analog out, 0.18V to 2.2V
- Illumination: Red ultra bright LED
- Sensing element: Directional photo transistor with 5 degree viewing angle
- Sensing distance: 9mm to 20mm from the surface
- Number of sensors: 3
- Distance between adjacent sensors: 18mm
- Connector: 16 pin FRC male connector
- Mounting: Four 3mm mounting holes
- 16 pin FRC cable included

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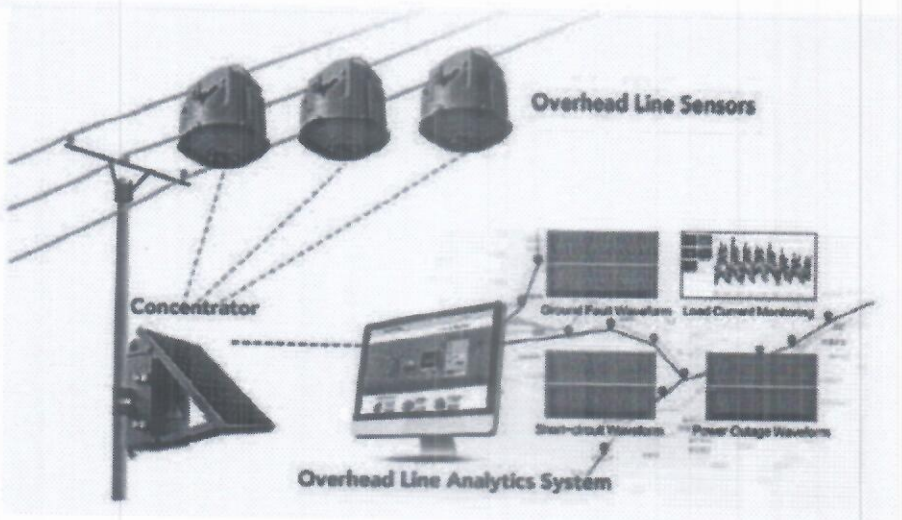


Fig.No.4.13 Line Analytics Sensor

4.8 Three Phase Contractor

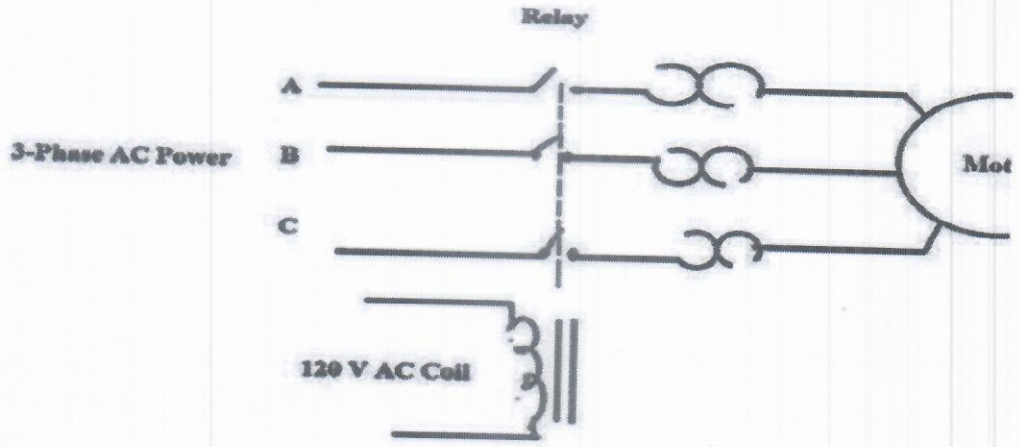
A contactor is one of the main electrical circuit parts, which can stand on its own power control de a starter. They are used to connect and break power supply lines running through power line establish and interrupt electrical power circuits. These are used in light loads, complex machine c used with motors, transformers, heaters. It can be considered as an intersection point between th and power circuit because it is controlled by the control circuit, it also controls the circuit betw loads. This article focuses on the importance of contactor in and electric field. What is Contactor? Definition: Contactors are electrically controlled switching devices which are used for switching basic operation of this is similar to a relay, but the only dierence is that contractors can car compared to relay up to 12500A. They cannot provide short circuit or overload protection bu contact when coil excites.

Construction of a Contactor

The contactor consists of two iron cores, where one is fixed and the other one is the movable insulated copper coil. Where the copper coil is located on the fixed core. There are six main co connection, where three are fixed cores and the other three

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are movable cores. These contacts pure copper, and the contact points are made from special alloy to withstand high start temperature. A spring which is located between coil and the movable core, auxiliary contacts it co open or closed. The main contacts cut on and o the light current loads such as contactors co and many other control circuit parts are linked to contact mechanism. A three-phase AC power su the circuit which is shown below,



Working Principle of Contactors An electromagnetic field is generated whenever current flows where the moving coils attract ea amount of current is drawn initially by an electromagnetic coil. The moving contact is pushed for core, as a result, the force created by the electromagnet holds the moving and fixed contacts toge On de-energizing, the contactor coil gravity or spring moves back the electro-magnetic position and there is no flow of current in the circuit. If contactors are energized with AC current, a small portion of the coil is the shaded magnetic flux in the core is slightly delayed. This effect is too average as it prevents buzzing at twice line frequency. There are internal tipping point processes to ensure rapid contactors can open and closed very rapidly. From the figure the supply is given using a switch, that is when the switch is closed through the contactor coil and attaches the moving

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core. The contactor attached to th closes and the motor starts running. When the switch is released the electromagnetic e arrangement pause the moving coil back to its initial position and power supply to the moment.

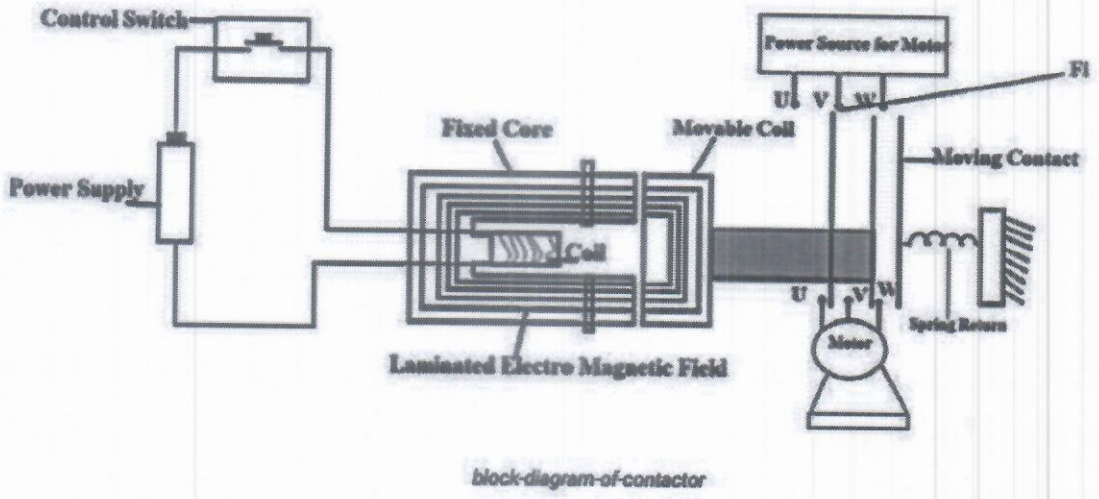


Fig.No.4.14 working of Contractor

4.9 Buzzer

4.9.1 General Description

A buzzer or beeper is an audio signaling device, which may be mechanical, electromechanical, or piezoelectric. Typical uses of buzzers and beepers include alarm devices, timers and confirmation of user input such as a mouse click or key stroke.

Buzzer is an integrated structure of electronic transducers, DC power supply, widely used in computers, printers, copiers, alarms, electronic toys, automotive electronic equipment, telephones, timers and other electronic products for sound devices. Active buzzer 5V Rated power can be directly connected to a

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continuous sound, this section dedicated sensor expansion module and the board in combination, can complete a simple circuit design, to "plug and play."

4.9.2 Product Description

A buzzer or beeper is an audio signalling device, which may be mechanical, electromechanical, or piezoelectric. Typical uses of buzzers and beepers include alarm devices, timers, and confirmation of user input such as a mouse click or keystroke.

It generates consistent single tone sound just by applying D.C voltage. Using a suitably designed resonant system, this type can be used where large sound volumes are needed. At Future Electronics we stock many of the most common types categorized by Type, Sound Level, Frequency, Rated Voltage, Dimension and Packaging Ty

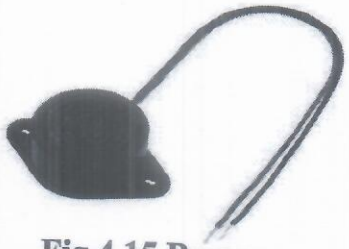


Fig.4.15 Buzzer

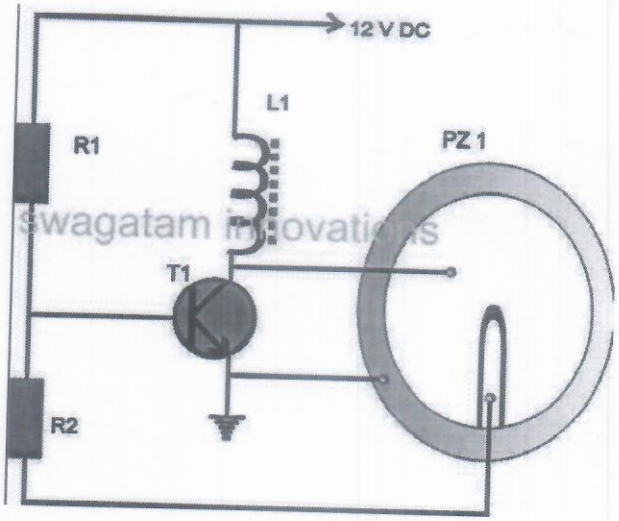


Fig. 4.14 Circuit diagram

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4.9.3 Features

- Input supply: 5 V_{DC}
- Current consumption: 9.0 mA max.
- Oscillating frequency: 3.0 ±0.5KHz
- Sound Pressure Level: 85dB min.

4.9.4 Application

- Confirmation of user input (ex: mouse click orkeystroke)
- Electronicmetronomes
- Sporting events
- Judging Panels

4.10 IOT

The Internet of Things is an emerging topic of technical, social, and economic significance. Consumer products, durable goods, cars and trucks, industrial and utility components, sensors, and other everyday objects are being combined with Internet connectivity and powerful data analytic capabilities that promise to transform the way we work, live, and play. Projections for the impact of IoT on the Internet and economy are impressive, with some anticipating as many as 100 billion connected IoT devices and a global economic impact of more than $11 trillion by 2025.

At the same time, however, the Internet of Things raises significant challenges that could stand in the way of realizing its potential benefits. Attention-grabbing headlines about the hacking of Internet-connected devices, surveillance concerns, and privacy fears already have captured public attention. Technical challenges remain and new policy, legal and development challenges are emerging.

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This overview document is designed to help the Internet Society community navigate the dialogue surrounding the Internet of Things in light of the competing predictions about its promises and perils. The Internet of Things engages a broad set of ideas that are complex and intertwined from different perspectives. Key concepts that serve as a foundation for exploring the opportunities and challenges of IoT include:

- **IoT Definitions:** The term Internet of Things generally refers to scenarios where network connectivity and computing capability extends to objects, sensors and everyday items not normally considered computers, allowing these devices to generate, exchange and consume data with minimal human intervention. There is, however, no single, universal definition.
- **Enabling Technologies:** The concept of combining computers, sensors, and networks to monitor and control devices has existed for decades. The recent confluence of several technology market trends, however, is bringing the Internet of Things closer to widespread reality. These include *Ubiquitous Connectivity*, *Widespread Adoption of IP-based Networking*, *Computing Economics*, *Miniaturization*, *Advances in Data Analytics*, and the *Rise of Cloud Computing*.
- **Connectivity Models**: IoT implementations use different technical communications models, each with its own characteristics. Four common communications models described by the Internet Architecture Board include: *Device-to-Device, Device-to-Cloud, Device-to-Gateway*, and *Back-End Data-Sharing*. These models highlight the flexibility in the ways that IoT devices can connect and provide value to the user.
- **Transformational Potential:** If the projections and trends towards IoT become reality, it may force a shift in thinking about the implications and

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issues in a world where the most common interaction with the Internet comes from passive engagement with connected objects rather than active engagement with content. The potential realization of this outcome – a "hyperconnected world" — is testament to the general-purpose nature of the Internet architecture itself, which does not place inherent limitations on the applications or services that can make use of the technology.

Five key IoT issue areas are examined to explore some of the most pressing challenges and questions related to the technology. These include security; privacy; interoperability and standards; legal, regulatory, and rights; and emerging economies and development.

- ***Security***

While security considerations are not new in the context of information technology, the attributes of many IoT implementations present new and unique security challenges. Addressing these challenges and ensuring security in IoT products and services must be a fundamental priority.Users need to trust that IoT devices and related data services are secure from vulnerabilities, especially as this technology become more pervasive and integrated into our daily lives. Poorly secured IoT devices and services can serve as potential entry points for cyber attack and expose user data to theft by leaving data streams inadequately protected.

The interconnected nature of IoT devices means that every poorly secured device that is connected online potentially affects the security and resilience of the Internet globally. This challenge is amplified by other considerations like the mass-scale deployment of homogenous IoT devices, the ability of some devices to automatically connect to other devices, and the likelihood of fielding these devices in unsecure environments.

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As a matter of principle, developers and users of IoT devices and systems have a collective obligation to ensure they do not expose users and the Internet itself to potential harm. Accordingly, a collaborative approach to security will be needed to develop effective and appropriate solutions to IoT security challenges that are well suited to the scale and complexity of the issues.

- ***Privacy***

The full potential of the Internet of Things depends on strategies that respect individual privacy choices across a broad spectrum of expectations. The data streams and user specificity afforded by IoT devices can unlock incredible and unique value to IoT users, but concerns about privacy and potential harms might hold back full adoption of the Internet of Things. This means that privacy rights and respect for user privacy expectations are integral to ensuring user trust and confidence in the Internet, connected devices, and related services.

Indeed, the Internet of Things is redefining the debate about privacy issues, as many implementations can dramatically change the ways personal data is collected, analyzed, used, and protected. For example, IoT amplifies concerns about the potential for increased surveillance and tracking, difficulty in being able to opt out of certain data collection, and the strength of aggregating IoT data streams to paint detailed digital portraits of users. While these are important challenges, they are not insurmountable. In order to realize the opportunities, strategies will need to be developed to respect individual privacy choices across a broad spectrum of expectations, while still fostering innovation in new technology and services.

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CHAPTER 5

SOFTWARE IMPLIMENTATION

5.1 About Embedded C

High-level language programming has long been in use for embedded-systems development. However, assembly programming still prevails, particularly for digital-signal processor (DSP) based systems. DSPs are often programmed in assembly language by programmers who know the processor architecture inside out. The key motivation for this practice is performance, despite the disadvantages of assembly programming when compared to high-level language programming.

If the video decoding takes 80 percent of the CPU-cycle budget instead of 90 percent, for instance, there are twice as many cycles available for audio processing. This coupling of performance to end-user features is characteristic of many of the real-time applications in which DSP processors are applied. DSPs have a highly specialized architecture to achieve the performance requirements for signal processing applications within the limits of cost and power consumption set for consumer applications. Unlike a conventional Load-Store (RISC) architecture, DSPs have a data path with memory-access units that directly feed into the arithmetic units. Address registers are taken out of the general-purpose register file and placed next to the memory units in a separate register file.

A further specialization of the data path is the coupling of multiplication and addition to form a single cycle Multiply-accumulate unit (MAC). It is combined with special-purpose accumulator registers, which are separate from the general-purpose registers. Data memory is segmented and placed close to the MAC to achieve the high bandwidths required to keep up with the streamlined data path. Limits are often placed on

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the extent of memory-addressing operations. The localization of resources in the data path saves many data movements that typically take place in a Load-Store architecture.

The most important, common arithmetic extension to DSP architectures is the handling of saturated fixed-point operations by the arithmetic unit. Fixed-point arithmetic can be implemented with little additional cost over integer arithmetic. Automatic saturation (or clipping) significantly reduces the number of control-flow instructions needed for checking overflow explicitly in the program.Changes in technological and economic requirements make it more expensive to continue programming DSPs in assembly. Staying with the mobile phone as an example, the signal-processing algorithms required become increasingly complex. Features such as stronger error correction and encryption must be added. Communication protocols become more sophisticated and require much more code to implement. In certain markets, multiple protocol stacks are implemented to be compatible with multiple service providers. In addition, backward compatibility with older protocols is needed to stay synchronized with provider networks that are in a slow process of upgrading.

Today, most embedded processors are offered with C compilers. Despite this, programming DSPs is still done in assembly for the signal processing parts or, at best, by using assembly-written libraries supplied by manufacturers. The key reason for this is that although the architecture is well matched to the requirements of the signal-processing application, there is no way to express the algorithms efficiently and in a natural way in Standard C. Saturated arithmetic.

For example, is required in many algorithms and is supplied as a primitive in many DSPs. However, there is no such primitive in Standard C. To express saturated arithmetic in C requires comparisons, conditional statements, and correcting assignments.

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Instead of using a primitive, the operation is spread over a number of statements that are difficult to recognize as a single primitive by a compiler.

5.1.1 Description

Embedded C is designed to bridge the performance mismatch between Standard C and the embedded hardware and application architecture. It extends the C language with the primitives that are needed by signal-processing applications and that are commonly provided by DSP processors. The design of the support for fixed-point data types and named address spaces in Embedded C is based on DSP-C. DSP-C [1] is an industry-designed extension of C with which experience was gained since 1998 by various DSP manufacturers in their compilers. For the development of DSP-C by ACE (the company three of us work for), cooperation was sought with embedded-application designers and DSP manufacturers.

The Embedded C specification extends the C language to support freestanding embedded processors in exploiting the multiple address space functionality, user-defined named address spaces, and direct access to processor and I/O registers. These features are common for the small, embedded processors used in most consumer products. The features introduced by Embedded C are fixed-point and saturated arithmetic, segmented memory spaces, and hardware I/O addressing. The description we present here addresses the extensions from a language-design perspective, as opposed to the programmer or processor architecture perspective.

5.2 Multiple Address Spaces

Embedded C supports the multiple address spaces found in most embedded systems. It provides a formal mechanism for C applications to directly access (or map onto) those individual processor instructions that are designed for optimal memory

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access. Named address spaces use a single, simple approach to grouping memory locations into functional groups to support MAC buffers in DSP applications, physical separate memory spaces, direct access to processor registers, and user-defined address spaces.

The Embedded C extension supports defining both the natural multiple address space built into a processor's architecture and the application-specific address space that can help define the solution to a problem.

Embedded C uses address space qualifiers to identify specific memory spaces in variable declarations. There are no predefined keywords for this, as the actual memory segmentation is left to the implementation. As an example, assume that **X** and **Y** are memory qualifiers. The definition:

X inta[25] ;

Means that **a** is an array of 25 integers, which is located in the **X** memory. Similarly (but less common):

X int * Y p ;

Means that the pointer **p** is stored in the **Y** memory. This pointer points to integer data that is located in the **X** memory. If no memory qualifiers are used, the data is stored into unqualified memory.

For proper integration with the C language, a memory structure is specified, where the unqualified memory encompasses all other memories. All unqualified pointers are pointers into this unqualified memory. The unqualified memory abstraction is needed to keep the compatibility of the **void *** type, the **NULL** pointer, and to avoid duplication of all library code that accesses memory through pointers that are passed as parameters.

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5.3 Named Register

Embedded C allows direct access to processor registers that are not addressable in any of the machine's address spaces. The processor registers are defined by the compiler-specific, named-register, storage class for each supported processor. The processor registers are declared and used like conventional C variables (in many cases volatile variables). Developers using Embedded C can now develop their applications, including direct access to the condition code register and other processor-specific status flags, in a high-level language, instead of inline assembly code.

Named address spaces and full processor access reduces application dependency on assembly code and shifts the responsibility for computing data types, array and structure offsets, and all those things that C compilers routinely and easily do from developers to compilers.

5.4 I/O Hardware Addressing

The motivation to include primitives for I/O hardware addressing in Embedded C is to improve the portability of device-driver code. In principle, a hardware device driver should only be concerned with the device itself. The driver operates on the device through device registers, which are device specific. However, the method to access these registers can be very different on different systems, even though it is the same device that is connected. The I/O hardware access primitives aim to create a layer that abstracts the system-specific access method from the device that is accessed. The ultimate goal is to allow source-code portability of device drivers between different systems. In the design of the I/O hardware-addressing interface, three requirements needed to be fulfilled:

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- The device-drive source code must be portable.
- The interface must not prevent implementations from producing machine code that is as efficient as other methods.
- The design should permit encapsulation of the system-dependent access method.

The design is based on a small collection of functions that are specified in the <iohw.h> include file. These interfaces are divided into two groups; one group provides access to the device, and the second group maintains the access method abstraction itself.

To access the device, the following functions are defined by Embedded C:

```
unsignedintiord( ioreg_designator );
voidiowr( ioreg_designator, unsigned int value );
voidioor( ioreg_designator, unsigned int value );
voidioand( ioreg_designator, unsigned int value );
voidioxor( ioreg_designator, unsigned int value );
```

These interfaces provide read/write access to device registers, as well as typical methods for setting/resetting individual bits. Variants of these functions are defined (with **buf** appended to the names) to access arrays of registers. Variants are also defined (with l appended) to operate with **long** values.

All of these interfaces take an I/O register designator **ioreg_designator** as one of the arguments. These register designators are an abstraction of the real registers provided by the system implementation and hide the access method from the driver source code. Three functions are defined for managing the I/O register designators. Although these are abstract entities for the device driver, the driver does have the obligation to initialize and release the access methods. These functions do not access or initialize the device itself

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because that is the task of the driver. They allow, for example, the operating system to provide a memory mapping of the device in the user address space.

voidiogroup_acquire(iogrp_designator);
voidiogroup_release(iogrp_designator);
voidiogroup_map(iogrp_designator, iogrp_designator);

The **iogrp_designator** specifies a logical group of I/O register designators; typically this will be all the registers of one device. Like the I/O register designator, the I/O group designator is an identifier or macro that is provided by the system implementation.The map variant allows cloning of an access method when one device driver is to be used to access multiple identical devices.

5.5 Embedded C Portability

By design, a number of properties in Embedded C are left implementation defined. This implies that the portability of Embedded C programs is not always guaranteed. Embedded C provides access to the performance features of DSPs. As not all processors are equal, not all Embedded C implementations can be equal For example, suppose an application requires 24-bit fixed-point arithmetic and an Embedded C implementation provides only 16 bits because that is the native size of the processor. When the algorithm is expressed in Embedded C, it will not produce outputs of the right precision.

In such a case, there is a mismatch between the requirements of the application and the capabilities of the processor. Under no circumstances, including the use of assembly, will the algorithm run efficiently on such a processor. Embedded C cannot overcome such discrepancies. Yet, Embedded C provides a great improvement in the portability and software engineering of embedded applications. Despite many differences between

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performance-specific processors, there is a remarkable similarity in the special-purpose features that they provide to speed up applications.

Writing C code with the low-level processor-specific support may at first appear to have many of the portability problems usually associated with assembly code. In the limited experience with porting applications that use Embedded C extensions, an automotive engine controller application (about 8000 lines of source) was ported from the eTPU, a 24-bit special-purpose processor, to a general-purpose 8-bit Freescale 68S08 with about a screen full of definitions put into a single header file. The porting process was much easier than expected. For example, variables that had been implemented on the processor registers were ported to unqualified memory in the general-purpose microprocessor by changing the definitions in the header definition and without any actual code modifications. The exercise was to identify the porting issues and it is clear that the performance of the special-purpose processor is significantly higher than the general-purpose target.

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CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

- In this report,an efficient method for transmission line breakage detection and alerting system is concluded and overcome the problem in transmission line.
- And also reduce time for identification of transmission breakage and fault occurring area.
- Cost wise in this system overcome the existing system.

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3. Title of the project : AUTOMATIC FAULT DETECTION AND LOCATION OF TRANSMISSION LINES USING IoT.

4. Project code : EEE - 177

It is certified that a sum of Rs. 7,500 (Rupees) Sanctioned by the council for carrying out above mentioned student project has been utilized for the purpose for which it was sanctioned and sum of Rs. NIL remaining unutilized is refunded.

Signature of the guide

Signature of the HOD

Signature of the
REGISTRAR/PRINCIPAL/DEAN
With SEAL

PRINCIPAL
T.J.S. ENGINEERING COLLEGE
PERUVOYAL, GUMMIDIPOONDI T.K.
(NEAR KAVARAIPETTAI)
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T.J.S.E.C.

PRINCIPAL
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